138/c

CS7T3

Reg. No.

eventh Semester B.E. Degree Examination, February 2002

Computer Science and Engineering

Advanced Computer Architecture

e: 3 hrs.] Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. Answers should be precise and specific.
3. Missing or improper data if any in the problems should be assumed suitably with proper justifications.

1. (a) Name the different parallel program models and explain the salient features of any one method in detail along with the relevant diagram and/or pseudo statements if any. **(6 Marks)**

(b) Discuss in brief how the following parameters contribute to evaluate the performance of parallel architectures.

i) Data transfer time.

ii) Overhead and occupancy

iii) Communication cost.

Give the performance relation in each case. **(8 Marks)**

(c) Differentiate among the following architectural classifications:

i) SISD ii) SIMD iii) MISD and iv) MIMD.

Draw the functional diagram of an SIMD machine and explain its working principles. **(6 Marks)**

2. (a) Draw and explain the following diagrams involving the following set of operations in an instruction execution phase.

i) Instruction fetch (I.F.) ii) Instruction Decode (I.D.)

iii) Operand Fetch (O.F.) iv) Execute (EX)

1) Diagram of a four stage pipeline processor involving the above 4-phases.

2) Time-space diagram (Pipelined)

Indicate all the four phases of execution clearly drawn on figures (1) and (2) respectively. **(10 Marks)**

(b) What do you mean by the logic carry save adders and carry propagate adders? Explain how they can be used to multiply two 8 bit fixed point numbers. Draw the appropriate pipelined tree diagram used for the purpose. **(10 Marks)**

3. (a) Define the following terms:

i) Latency ii) Latency sequence

iii) Average latency iv) Forbidden latency

v) Minimum achievable latency **(6 Marks)**

(b) A certain dynamic pipeline with 4 segments $S_1, S_2, S_3 \& S_4$ is characterised by the following r ervation table.

	t_0	t_1	t_2	t_3	t_4	t_5	t_6
S_1	X					X	
S_2			X				X
S_3		X		X			
S_4			X		X		

Contd... 2

4. (a) Considering the example of the ocean study problem, show that when the problem is scaled up and the processing system is fixed, the compute load per processor increases, but the communication load per unit time decreases. **(10 Marks)**

(b) What are microbenchmarks? Give an example and discuss how it could be useful in performance evaluation. **(10 Marks)**

5. (a) Explain the MSI or MESI cache coherency ensuring protocol. **(10 Marks)**

(b) In a bus based three processor system, the following instructions are executed by the processors :

Processor A	Processor B	Processor C
u=A	C=1	B=1
v=B	A=1	w=C

Assume at entry, u,v,w, A,B, and C are all initialised to zero. After executing all the instruction, it is found :

u=1, v=0 and w=0.

Show that these results do not satisfy the sequential consistency requirement. **(10 Marks)**

6. (a) Techniques like message passing using physical DMA or dedicated message processing as done in intel paragon system are used among others for obtaining highly scalable systems. Explain any one such message passing systems. **(10 Marks)**

(b) When systems are scaled up, processor cost and memory cost increase linearly with the no. of nodes n, while the switching network cost increases roughly as $n \log_2 n$. Assuming in a 64 processor system, the cost is equally divided between processors, memory and interconnection networks, find the ratios of this cost division when the no. of nodes is increased to 8192 from 64. **(10 Marks)**

7. (a) Discuss the significant properties of static interconnecting networks for parallel processors. In the light of these properties, evaluate the performance of n-dimensional hyper cubes. **(10 Marks)**

(b) Indicate a non-blocking switching network for handling the interconnection of 4 computing nodes, using 2 x 2 switches.

In your network, show how you would simultaneously establish the following interconnection without blocking ?

Processor A output to Proe. D input
Processor B output to Proc. A input
Processor C output to Proc. B input
Processor D output to Proc. C input **(10 Marks)**

8. (a) What is RAID? Describe any good RAID system you know. **(10 Marks)**

(b) Write notes on any ONE :

i) Different steps in parallelisation of a problem and the goals of each of these steps.

OR

ii) Shared address space primitives :

CREATE, LOCK, BARRIER, WAIT-FOR-END. **(10 Marks)**

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USN

Seventh Semester B.E. Degree Examination, January/February 2005

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Is parallel computing inevitable ? Explain its need in terms of application, technology of architectural trends. (10 Marks)

   (b) Briefly explain three parallel architecture models and compare their merits and demerits. (10 Marks)

2. (a) What are the design issues of pipeline arechitecture ? Explain how feedback in pipeline enhance the speed up ? Illustrate this by taking an example of adding 8 floating point numbers. (10 Marks)

   (b) What is systolic array ? How is it associated with pipeline structure ? Explain systolic array structure for matrix multiplication. (10 Marks)

3. (a) Explain the following operations on instruction pipeline structure.
   a) Optimisation of number of stages of pipeline
   b) Collisions (10 Marks)

   (b) How super scalar processing is fast compared to parallel processors ? Explain the characteristics of a super scalar processor. Explain the concept of dynamic instruction scheduling. (10 Marks)

4. (a) What are 4 stages of parallelisation process? Explain each of the stages with suitable example. (10 Marks)

   (b) $\pi = \int_0^1 \frac{4}{1+x^2} . dx$

   To solve π value. Explain how parallel system can be designed. (10 Marks)

5. (a) Why scaling of parallel architecture is important ? Explain problem constrained, time- constrained and memory-constrained scaling. Mention their speed up. (10 Marks)

   (b) What are metrics used for measuring the performance of system. Explain the performance parameters. (10 Marks)

6. (a) How bus snooping can be used to avoid the cache coherence ? What are demerits of this strategy ? (10 Marks)

   (b) Explain point to point synchronisation and global event synchronisation. (10 Marks)

7. (a) Explain any three routing mechanisms. (10 Marks)

   (b) What is meant by flow control in inter connection networks. Compare link level flow control and end to end flow control. (10 Marks)

8. Write short notes on :
   a) Fault tolerance
   b) Data - flow architecture
   c) Daisy chaining
   d) Memory consistency (5×4=20 Marks)

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USN

Seventh Semester B.E. Degree Examination, January/February 2004

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs.] [Max.Marks : 100

Note: 1. *Answer any FIVE full questions.*
2. *All questions carry equal marks.*

1. (a) Discuss the evolution of parallel computing architecture from
   i) Technology point of view and ii) Application point of view. (10 Marks)

   (b) In a single processor computing system. the processor-cache subsystem is connected to the main memory system through a bus with a 64 bit data path. In case of a read miss in the cache, the processor takes 2 clocks (the processor clock is at 40 MHz) to present the address on the bus and the memory takes 100ns access time. If the cache line size is 32 bytes. compute the latency for a read miss: What is bandwidth obtained on this transfer ? (10 Marks)

2. (a) Discuss the factors that could cause a delay in the instruction pipe. Indicate methods adopted to reduce these delays. (10 Marks)

   (b) Consider the 4 stage pipe line with a reservation table as shown in fig Q2.b.

$t \rightarrow$	1	2	3	4	5	6	7	8
S_1	X						X	
S_2		X	X			X		
S_3				X				
S_4					X			X

Reservation Table fig. Q2.b

   (b) Find the minimum average latency cycle for the pipeline.
   What is the corresponding throughput if the pipe line is continuously operated at 40 MHz clock?
   What is the best throughput possible if delays are used to obtain optimum performance of the pipe line? (10 Marks)

3. (a) In a super market, vendors would be interested in extracting the information on the item-sets, the customers frequently purchase. Using the large database, indicating the set of items purchased by the customers in each purchase transaction. show how this information of frequently purchased item sets could be obtained. Expose the parallelism that exists in the process. (10 Marks)

   (b) With a suitable example explain the need for lock operation in a bus based shared memory multiprocessor system. Give a good subroutine for realising the Lock, considering the existence of Cache-coherecy protocols in the system. Explain the operation of the subroutine. (10 Marks)

Contd.... 2

USN

Seventh Semester B.E. Degree Examination, June 2003

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs. [Max.Marks : 100

Note: 1. *Answer any FIVE full questions.*

1. (a) Distinguish between the sequential and parallel computing architectures. Mention the performance model of the parallel computing system with reference to the sequential architecture. (10 Marks)

   (b) Briefly discuss the design issues of three parallel computing structures. (10 Marks)

2. (a) 50 floating point numbers are to be summed using a 4-stage pipeline with an extra register and a suitable feedback through multiplexers at the input. Indicate the arrangement for doing this, giving the register and multiplexer controls required at the beginning, in the middle and end of process. Compute the time required for obtaining sum interms of clock pulses. (8 Marks)

   (b) A certain dynamic pipeline with 3 segments $S1$, $S2$ & $S3$ is characterised by the following reservation table.

	1	2	3	4	5	6	7	8
S_1	X					X		X
S_2		X		X				
S_3			X		X		X	

   Determine (i) Forbidden list

   (ii) Collision vector

   (iii) Transition diagram

   (iv) Greedy cycle and MAL

   (v) Throughput (12 Marks)

3. (a) Explain Data orchestration under message passing for the case of equation solver example. Also write the pseudo code for the same. (12 Marks)

   (b) Briefly explain Red-black ordering that can be used in decomposition step of parallelisation. Also list its advantages and disadvantages. (8 Marks)

4. (a) Explain why workload driven evaluation for multiprocessor architecture is more difficult than for uniprocessor system. (10 Marks)

   (b) Describe the characteristics of workload driven evaluation (10 Marks)

5. (a) What is cache-coherence problem? Explain a method to eliminate it. (10 Marks)

   (b) Explain the below software lock algorithm, along with performance comparison.

   (i) Test and set lock with Back off

Cont../d.... 2

4. (a) Considering the example of the ocean study problem, show that when the problem is scaled up and the processing system is fixed, the compute load per processor increases, but the communication load per unit time decreases. (10 Marks)

   (b) What are microbenchmarks? Give an example and discuss how it could be useful in performance evaluation. (10 Marks)

5. (a) Explain the MSI or MESI cache coherency ensuring protocol. (10 Marks)

   (b) In a bus based three processor system, the following instructions are executed by the processors :

Processor A	Processor B	Processor C
u=A	C=1	B=1
v=B	A=1	w=C

   Assume at entry, u,v,w, A,B, and C are all initialised to zero. After executing all the instruction, it is found :

   u=1, v=0 and w=0.

   Show that these results do not satisfy the sequential consistency requirement. (10 Marks)

6. (a) Techniques like message passing using physical DMA or dedicated message processing as done in intel paragon system are used among others for obtaining highly scalable systems. Explain any one such message passing systems. (10 Marks)

   (b) When systems are scaled up, processor cost and memory cost increase linearly with the no. of nodes n, while the switching network cost increases roughly as $n \log_2 n$. Assuming in a 64 processor system, the cost is equally divided between processors, memory and interconnection networks, find the ratios of this cost division when the no. of nodes is increased to 8192 from 64. (10 Marks)

7. (a) Discuss the significant properties of static interconnecting networks for parallel processors. In the light of these properties, evaluate the performance of n-dimensional hyper cubes. (10 Marks)

   (b) Indicate a non-blocking switching network for handling the interconnection of 4 computing nodes, using 2 x 2 switches.

   In your network, show how you would simultaneously establish the following interconnection without blocking ?

   Processor A output to Proe. D input
   Processor B output to Proc. A input
   Processor C output to Proc. B input
   Processor D output to Proc. C input (10 Marks)

8. (a) What is RAID? Describe any good RAID system you know. (10 Marks)

   (b) Write notes on any ONE :

   i) Different steps in parallelisation of a problem and the goals of each of these steps.

   OR

   ii) Shared address space primitives :

   CREATE, LOCK, BARRIER, WAIT-FOR-END. (10 Marks)

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138/c

CS7T3

Reg. No.

Seventh Semester B.E. Degree Examination, January/February 2003

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs.] [Max. Marks: 100

Note: 1. *Answer any FIVE full questions.*
2. *Be Brief and relevant in your answers.*

(a) Bring out the technology and application aspects that speeded up the parallel processing architecture development. (10 Marks)

(b) A particular program has the following feature :
21% of the program can be worked out in parallel by 7 processors -
60% by 3 processors in parallel
and 19% has to be done sequentially.

If there is no other parallelism in the program, calculate the speed up possible if the program is handled by

i) a 2 - processor system

ii) a 4 - processor system

iii) an 8 - processor system. (10 Marks)

2. (a) What do you understand by pipe lined instruction execution? Explain the various factors that cause delay in the instruction pipelines. (10 Marks)

(b) With a diagram, explain a systolic array and its operation for a 2×2 matrix multiplication. (10 Marks)

3. (a) Taking the example of the ocean current study problem, explain the distinct steps in executing a problem with a large parallelism inherent in it, using a system with a large number processors operating in parallel. (10 Marks)

(b) Give the equation solver Kernel program associated with ocean current studies for being worked out in an SIMD environment. (10 Marks)

4. (a) Discuss with examples, the rolls of

i) Micro bench marks.

ii) Kernel programs in evaluating the performance of processing systems. (10 Marks)

(b) Three SPEC bench marks run on 2 processor systems A and B gave the following results :

	Time for SPEC Prog. 1	Time for SPEC Prog.2	Time for SPEC Prog 3
SYSTEM A:	2 secs.	15secs.	20 Secs.
SYSTEM B:	3 secs.	8secs.	25 Secs.

If the anticipated work load by a user organisation is 30% of programs of SPEC prog 1 type, 50% SPEC prog 2 type and 20% SPEC prog 3 type, which system would be preferable from work load point of view of for the organization. (5 Marks)

(c) Discuss the formal procedure for evaluating a real machine. (5 Marks)

Contd.... 2

5. (a) What is cache coherence? Explain the concept of bus snooping by cache controllers to maintain coherence. (12 Marks)

(b) State the conditions sufficient to ensure sequential consistency in a bus based parallel processor system with individual cache on each processor and a global memory.

Three parallel processors in such a system have programs as indicated below :

Proc. 1	Proc 2	Proc 3
Prog : A=1	Prog : u=A	Prog : B = 1
dce B	w=B	V = B
B = A		Print u,v,w.

Assume initially all variables are zero and the print out obtained is 1,0,1 for u,v,w. Is the result sequentially consistent? If yes, give a global sequence of execution of these instructions that could produce this result. (8 Marks)

6. (a) Explain the scalability of parallel processing systems and indicate the desirable properties of scalable systems in terms of band width of interconnection systems, latency, cost and packaging aspects. (10 Marks)

(b) With a block diagram explain a scalable processor system with shared memory and DMA based data transfer through the interconnection network. (10 Marks)

7. (a) Describe the hypercube interconnection network and evaluate its performance in terms of useful features from parallel processing point of view. (12 Marks)

(b) Show an 8×8 omega interconnection network using 2×2 switch array. Check if the network blocks the simultaneous interconnections specified below: (8 Marks)

$$\begin{matrix} Input \\ Output \end{matrix} \begin{pmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 1' & 7' & 4' & 2' & 6' & 0' & 3' & 5' \end{pmatrix}$$

8. Write short notes on any FOUR : (4×5=20 Marks)

i) Convergence of parallel architectures.

ii) Clusters and networks of work stations.

iii) Super scaler processing

iv) Pipelined integer multipliers

v) Dedicated message processing architecture.

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1258/c

CS7T3

Reg. No.

Seventh Semester B.E. Degree Examination, July/August 2002

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs.] [Max Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Define a parallel computer. Briefly describe the trends that have caused the development of parallel architecture. (10 Marks)
   (b) Describe the shared memory multiprocessor systems. (5 Marks)
   (c) Mention the fundamental design issues of parallel architectures. Explain the two types of synchronizations required by parallel programs. (5 Marks)
2. (a) What is meant by pipeline processing? Give the design of a floating point adder with four stages. (10 Marks)
   (b) Describe a Wallace tree. (5 Marks)
   (c) Show how a systolic array can be used for the multiplication of two 3×3 matrices. (5 Marks)
3. (a) Describe the steps involved in creating a parallel program. (10 Marks)
   (b) Explain the red-black ordering technique for Equation Solver. (5 Marks)
   (c) List the basic message passing primitives with their functions. (5 Marks)
4. (a) Discuss the need for scaling of workloads. Describe the different scaling models of workloads and the speed up measures. (10 Marks)
   (b) List the types of microbenchmarks used for parallel systems and their applications. (5 Marks)
   (c) Define the metrics used to characterize the performance of parallel machines. (5 Marks)
5. (a) Illustrate the Cache coherence problem and suggest a method of solving it. (10 Marks)
   (b) What is meant by sequential consistency? What are the sufficient conditions for preserving sequential consistency? (5 Marks)
   (c) Describe the components of a synchronisation event. What are the choices for waiting algorithms? (5 Marks)
6. (a) What is meant by scalable systems? Describe the requirments of scaling. (10 Marks)
   (b) Mention the important issues in Network transactions. (5 Marks)
   (c) Explain the physical DMA. (5 Marks)
7. (a) Discuss the different possibilities for interconnection networks. Distinguish between synchronous and asynchronous buses. (10 Marks)
   (b) What is meant by bus arbitration? Explain Daisy Chaining. (5 Marks)

Contd.... 2

   (c) What are multistage interconnection networks? Draw an 8 × 8 Omega network. (5 Marks)
8. Write explanatory notes on:
   (a) Fault tolerance
   (b) R A I D
   (c) Flynn's classification
   (d) Dataflow architectures (4×5=20 Marks)

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CS7T3

USN

Seventh Semester B.E. Degree Examination, January/February 2005

Computer Science and Engineering

Advanced Computer Architecture

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Is parallel computing inevitable ? Explain its need in terms of application, technology of architectural trends. (10 Marks)

   (b) Briefly explain three parallel architecture models and compare their merits and demerits. (10 Marks)

2. (a) What are the design issues of pipeline arechitecture ? Explain how feedback in pipeline enhance the speed up ? Illustrate this by taking an example of adding 8 floating point numbers. (10 Marks)

   (b) What is systolic array ? How is it associated with pipeline structure ? Explain systolic array structure for matrix multiplication. (10 Marks)

3. (a) Explain the following operations on instruction pipeline structure.
   a) Optimisation of number of stages of pipeline
   b) Collisions (10 Marks)

   (b) How super scalar processing is fast compared to parallel processors ? Explain the characteristics of a super scalar processor. Explain the concept of dynamic instruction scheduling. (10 Marks)

4. (a) What are 4 stages of parallelisation process? Explain each of the stages with suitable example. (10 Marks)

   (b) $\pi = \int_0^1 \frac{4}{1+x^2}.dx$

   To solve π value. Explain how parallel system can be designed. (10 Marks)

5. (a) Why scaling of parallel architecture is important ? Explain problem constrained, time- constrained and memory-constrained scaling. Mention their speed up. (10 Marks)

   (b) What are metrics used for measuring the performance of system. Explain the performance parameters. (10 Marks)

6. (a) How bus snooping can be used to avoid the cache coherence ? What are demerits of this strategy ? (10 Marks)

   (b) Explain point to point synchronisation and global event synchronisation. (10 Marks)

7. (a) Explain any three routing mechanisms. (10 Marks)

   (b) What is meant by flow control in inter connection networks. Compare link level flow control and end to end flow control. (10 Marks)

8. Write short notes on :
   a) Fault tolerance
   b) Data -flow architecture
   c) Daisy chaining
   d) Memory consistency (5×4=20 Marks)

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USN

CS-82

NEW SCHEME

Eighth Semester B.E.Degree Examination, May / June 2006
Computer Science Engineering
Advanced Computer Architecture

Time: 3 hrs.] [Max. Marks:100

Note: 1. *Answer any FIVE full questions.*

1 With generic diagrams, discuss the architecture and operation of the following:
   i. Shared memory multiprocessor systems.
   ii. MIMD systems.
   iii. Vector supercomputers. **(20 Marks)**

2 a. Consider the following sequence of instruction :

```
MOV R1, R2    ; R1 goes to R2
ADD R3, R2    ; (R3+R2) goes to R2
ADD R3, R4    ; (R3+R4) goes to R4
STORE R4, M2  ; R4 goes to memory at M2
STORE R2, M1  ; R2 goes to memory at M1
MOV R6, R4    ; R6 goes to R4.
```

The processor executing these instructions takes two instructions of the given sequence at a time and executes them simultaneously subject to data and resource dependences. In case it is not possible to execute both, it executes the first of the two instructions and tries to execute the second instruction in the next time slot with the instruction next in the sequence of instructions. Instructions are thus taken two at a time and executes simultaneously if possible. Consider each instruction takes two clocks.

How many clocks would the processor need to execute all the six instructions as given above?

By changing the sequence of instructions can you improve the performance? What is the best sequence and what is the corresponding clock period for the above program segment of six instructions? **(10 Marks)**

b. Compare the control flow and data flow architectures. Which architecture would expose parallelism to greater extent? **(10 Marks)**

3 a. Consider a 10-dimensional hypercube interconnecting network.
   i. How many process or nodes can it support?
   ii. How many links does it have?
   iii. Assuming the data travels by the shortest path, work out the number of links a data has to pass to move from any node to the farthest node.
   iv. Indicate a minimum link path to reach from node 2D3 hex to node 2E5 hex. **(10 Marks)**

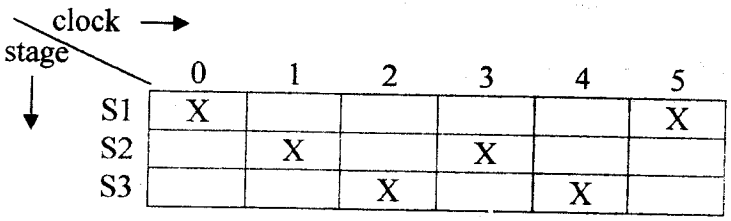
Contd...2

b. Indicate the various causes for stalling in the instruction pipe lines. Give some id about reducing such stalling. (10 Mar

4 a. In respect of back plane buses, discuss any two methods used for bus arbitration bus masters. (10 Mar

b. For the given non-linear pipe line with the reservation table below, find the minimu average latency cycle, and also the minimum constant latency cycle. If delay can b added, state what can be the maximum throughput possible from the pipe lin (10 Mark

Reservation table for the pipe line.



5 a. In connection with instruction pipe lines explain with adequate details the following:
i. Dynamic instruction scheduling.
ii. Branch handling techniques. (12 Marks)

b. Describe a pipelined floating point adder unit. (08 Marks)

6 a. With a diagram, explain the operation of a 8 x 8 baseline network using Z x Z switch units. (10 Marks)

b. Explain the MESI protocol for maintaining cache coherence in a multiprocessor system with each processor having its own cache. (10 Marks)

7 a. Explain how you would organize the solution of the simultaneous linear equation $A\underline{X} = \underline{B}$ with n unknowns, using a shared memory multiprocessor system with n/4 processors. (10 Marks)

b. Explain the different steps like decomposition assignment etc. to exploit parallelism of a problem for execution by a set of parallel processors. (10 Marks)

8 a. Consider a single processor is able to solve a set of simultaneous linear equations in 1000 variables in one minute, and has just enough memory for this operation, using a process with a time complexity proportional to the cube of the number of variables. Calculate assuming ideal conditions:
i. What size of problem can be handled by 900 such processors working in parallel and taking one minute for execution?
ii. What would be the memory constrained size of the problem?
iii. How much time would the problem of (ii) above take? (10 Marks)

b. Write short notes on:
i. Parallelizing the ray tracing problem.
ii. VLIW architecture. (10 Marks)

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CS82

USN

NEW SCHEME

Eighth Semester B.E. Degree Examination, Dec.06 / Jan.07
Computer Science and Engineering
Advanced Computer Architecture

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Give the Flynn's classification of computer architecture and hence describe the different architectures with neat block diagrams. **(14 Marks)**

b. A Workstation uses a 15 MHz processor with a claimed 10 MIPs rating to execute a given program mix. Assume a one cycle delay for each memory access.

i) What is the effective CPI of this computer?

ii) Suppose the processor is being upgraded with a 30 MHz clock. However the speed of memory subsystem remains same and consequently two clock cycles are needed for one memory access. If 30% of the instructions require one memory access per instruction, and another 5% require two memory access per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix? **(06 Marks)**

2 a. Define the following terms with examples : i) Flow dependence ii) Anti dependence iii) Output dependence iv) Control dependence v) Bernstein conditions. **(10 Marks)**

b. Consider the execution of the following code segment consisting of seven statements. Use Bernsteins conditions to detect the maximum parallelism embedded in the code. Justify the portions that can be executed in parallel and remaining portions that must be executed sequentially. Rewrite the code using parallel constructs 'Co begin' and 'Co end'.

S 1 : A = B + C
S 2 : C = D + E
S 3 : F = G + E
S 4 : C = A + F
S 5 : M = G + C
S 6 : A = L + C
S 7 : A = E + A. **(10 Marks)**

3 a. Compare and contrast RISC and CISC processors. **(10 Marks)**

b. Consider the following three interleaved memory design for a main memory system with 16 memory modules. Each module is assumed to have a capacity of 1 M byte. The machine is byte addressable.

Design 1 : 16 – way interleaving with one memory bank.
Design 2 : 8 - way interleaving with two memory banks
Design 3 : 4 - way interleaving with four memory banks
Design 4 : 2 - way interleaving with eight memory banks.

i) Specify the address format for each of the above memory organizations

ii) Determine the maximum memory bandwidth obtained if only one memory module fails in each of the above memory organizations.

iii) Comment on the relative merits of the different inter leaved memory organizations. **(10 Marks)**

Contd...2

4 a. Describe the 1 EEE 754 floating point standard for 32 bit floating point numbers. How are the primitive floating point arithmetic operations defined. **(10 Marks)**

b. Consider the following pipe line reservation table.

	1	2	3	4
S 1	X			X
S 2		X		
S 3			X	

i) List the set of forbidden latencies and initial collision vector.
ii) Draw the state transition diagram.
iii) List all simple cycles and greedy cycles.
iv) Determine the optimal content latency cycle and minimal average latency.
v) Let the pipeline clock period be τ =20 n secs. Determine the through put of this pipeline. **(10 Marks)**

(10 Marks)

5 a. Explain the following terms :
i) Store and forward routing at packet level.
ii) Virtual channels Vs physical channels
iii) Buffer deadlock Vs physical deadlocks
iv) Discard and Retransmission flow control
v) Virtual networks and sub networks.

b. i) Draw a 8 input Omega network using 2 x 2 switches. (10 Marks)
ii) Show the switch settings for routing a manage from node '101' to node '010' and from node '011' to node '100' simultaneously. Does flocking exist in this case.
iii) Determine how many permutations can be implemented in one pass through this network. What is the percentage of one pass permutations among all permutations.

6 a. Discuss the different steps in the parallelization process in detail. **(10 Marks)**

b. Write the pseudo code for parallel equation solver Kernal with decomposition into grid points and no explicit assignments. Describe the same. **(10 Marks)**

7 a. With the help of a neat figure describe the critical layers of abstractions and the aspects of system design that realize each of the layers. **(10 Marks)**

b. Describe the protocol to realize the shared address space communication abstraction. **(10 Marks)**

8 Write short note on :
a. Hardware and Software parallelism
b. IEEE Future bus and standard
c. Asynchronous and Synchronous linear pipeline models.
d. Hierarchical Bus systems. **(20 Marks)**

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CS82

USN

NEW SCHEME

Eighth Semester B.E. Degree Examination, May 2007
Computer Science
Advanced Computer Architecture

Time: 3 hrs.] [Max. Marks:100

Note : *1. Answer any FIVE full questions.*
2. Support the answers with relevant neat block diagram / timing diagram.

1 a. With neat block diagrams, explain the Flynn's classification of computer architecture. **(08 Marks)**

b. With neat generic block diagrams, explain any two shared-memory multiprocessor models. **(08 Marks)**

c. A 40 MHz processor was used to execute a bench mark program with the following instruction mix and clock cycle counts:

Instruction	Instruction count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program. **(04 Marks)**

2 a. Explain the terms flow dependence, antidependence and output dependence. **(06 Marks)**

b. Consider the following code fragment:

```
S1:  Load R1, A;      // R1 ← [A]
S2:  Add R2, R1;      // R2 ← [R1] + [R2]
S3:  Move R1, R3;     // R1 ← [R3]
S4:  Store B, R1;     // B ← [R1]
```

Indicate the types of data dependence present across the different statement and hence draw the data dependence graph. **(06 Marks)**

c. Discuss any one scheme of connection network that implements all communication patterns based on program demands. **(08 Marks)**

3 a. Draw the block diagram of a typical super scalar processor architecture consisting of an integer unit and a floating point unit and explain the salient features of super scalar processor of degree m = 2. **(10 Marks)**

b. With a neat block diagram, explain the c-access interleaved memory organization which allows block access in a pipelined fashion. Also sketch the timing chart indicating the major and minor cycle time. **(10 Marks)**

Contd.... 2

4 a. For the reservation table of a non-linear pipeline shown below:

	1	2	3	4	5	6
S1	X				X	
S2			X			
S3		X		X		X

i) Determine the Forbidden latency set and initial collision vector.
ii) Draw the state transition diagram.
iii) List all simple cycles and greedy cycles.
iv) Determine MAL. **(10 Marks)**

b. With an example differentiate between CSA and CPA adders. Design a pipeline unit for fixed-point multiplication of 8-bit integers using CSA tree. **(10 Marks)**

5 a. With a neat schematic block diagram, explain the design of a cross-point switch in a cross bar network. Indicate atleast one advantage and a limitation of cross bar network. **(10 Marks)**

b. Discuss the cache coherence problem. Explain the snoopy bus protocol used to achieve data consistency among the caches and shared memory. **(10 Marks)**

6 a. Describe how a sequential program can be converted into parallel program. **(08 Marks)**

b. Write the pseudocode for the data parallel equation solver kernel and explain. **(08 Marks)**

c. Highlight the need of BARRIER and LOCK primitive in solver kernel. **(04 Marks)**

7 a. What is meant by scalable system? Explain the requirements it places on a system design interms of bandwidth, latency and cost. **(10 Marks)**

b. With diagram, explain any one message passing protocols. Mention the advantages and disadvantages of it. **(10 Marks)**

8 Write short notes on:
a. Hardware parallelism and software parallelism
b. Message routing scheme
c. VLIW architecture
d. Branch handling technique. **(20 Marks)**

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CS82

Eighth Semester B.E. Degree Examination, May / June 08
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With neat diagram, discuss the operation of vector super computers. **(08 Marks)**

b. Write system attributes, which affects performance factors of the system. **(04 Marks)**

c. Consider the execution of an object code with 200,000 instructions on a 40 MHz processor. The program consists of 4 major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. **(08 Marks)**

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

i) Find total number of cycles required to execute the program.
ii) Calculate the average CPI when the program is executed on uniprocessor.
iii) Calculate MIPS rate.

2 a. Consider the following sequence of instruction.

1.	a : = 1	10.	j : = e × f
2.	b : = 2	11.	k : = d × f
3.	c : = 3	12.	*l* : = j × k
4.	d : = 4	13.	m : = 4 × *l*
5.	e : = 5	14.	n : = 3 × m
6.	f : = 6	15.	o : = n × i
7.	g : = a × b	16.	p : = o × h
8.	h : = c × d	17.	q : = p × q
9.	i : = d × e		

[NOTE : Nodes 1 to 6 takes one cycle to address and six cycles to fetch from memory. All remaining nodes (7 to 17) require 2 cycles to complete. Access time from nodes 7, 8, 9, 10, 11, 14 is 4. Access time from nodes 12, 13, 15, 16 is 3.] **(10 Marks)**

i) Write fine grain program graph for above code.
ii) Write coarse grain program graph by packing fine grain.
iii) Discuss how packing of grain improves performance (consider two processor).

b. With neat diagram, explain the operation of tagged token data flow computer. **(10 Marks)**

3 a. Define different types of data dependencies. **(05 Marks)**

b. With a neat diagram, explain low-order m – way interleaved memory organization. Write the timing chart indicating the major and minor cycle time. **(10 Marks)**

c. Differentiate between CISC and RISC architecture. **(05 Marks)**

4 a. For the reservation table of a non linear pipeline shown below :

	1	2	3	4	5	6
S_1	X					X
S_2		X			X	
S_3			X			
S_4				X		
S_5		X				X

i) What are the forbidden latencies? Write initial collision vector.
ii) Draw the state transition diagram.
iii) List all simple cycles and greedy cycles
iv) Determine MAL. **(10 Marks)**

b. Explain prefetch buffer and Internal Data Forwarding mechanisms used in instruction pipelining. **(10 Marks)**

5 a. Design arithmetic pipeline unit for fixed point multiplication of 8 bit integer using CSA and CPA. **(10 Marks)**

b. Design 8 × 8 omega network using 2 × 2 switch modulus and perfect shuffle. Explain data routing technique. **(10 Marks)**

6 a. What is cache coherence problem? Explain the good man's write once cache coherence protocol with state transition graph. **(10 Marks)**

b. What is Hot – spot problem? Explain the methods used to eliminate this problem. **(10 Marks)**

7 a. Discuss the case study of parallel programming application, simulating ocean current. **(10 Marks)**

b. Explain the different steps to exploit parallelism of a problem for execution by a set of parallel processors. **(10 Marks)**

8 Write short notes on:
a. Convergence division
b. VLIW architecture
c. Hazards avoidance
d. Daisy – chain bus arbitration. **(20 Marks)**

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2002 SCHEME

CS82

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Eighth Semester B.E. Degree Examination, June-July 2009
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With block diagrams, explain the Flynn's classification of computer architecture. **(10 Marks)**

b. Explain with diagram the operational model of SIMD super computer. **(10 Marks)**

2 a. Explain the Bernstein's conditions for parallelism. Detect the parallelism in the following code using Bernstein's conditions. (Assume no pipelining)

$P_1: C=D\times E$; $P_2: M=G+C$; $P_3: A=B+C$

$P_4: C=L+M$; $P_5: F=G\div E$ **(08 Marks)**

b. Define the following terms:

i) Granularity.

ii) Latency. **(04 Marks)**

iii) Grain packing and scheduling. **(08 Marks)**

c. Compare control flow and data flow architectures. **(10 Marks)**

3 a. Distinguish between typical RISC and CISC process architectures. **(10 Marks)**

b. Explain memory interleaving in detail.

4 a. For the given non-linear pipeline with the reservation table given below:

	0	1	2	3	4	5
S_1	X					X
S_2		X		X		
S_3			X		X	

i) Determine the forbidden latency set and initial collision vector.

ii) Draw state transition diagram.

iii) Latency cycles.

iv) Minimum constant latency.

v) Minimum average latency. **(12 Marks)**

b. Describe the IEEE754 floating point standard for 32-bit floating point number. How are the primitive floating point arithmetic operations defined? **(08 Marks)**

5 a. With the neat schematic block diagram, explain the design cross point switch in a cross bar network. **(10 Marks)**

b. Explain the cache coherence problem. Discuss the snoopy bus protocol used to achieve data consistency among caches and shared memories. **(10 Marks)**

6 a. Explain the different steps to exploit the parallelism of a problem for execution by a set of parallel processors. **(10 Marks)**

b. Write a pseudocode for the data parallel equation solver kernel and explain. **(10 Marks)**

7 a. What is meant by scalable system? Explain the requirements it places on a system design in terms of bandwidth, latency and cost. **(10 Marks)**

b. Describe the protocol to realize the shared address space communication abstraction. **(10 Marks)**

8 Write a short note on:

a. Hardware and software parallelism.

b. Asynchronous and synchronous pipeline model.

c. Branch handling techniques. **(20 Marks)**

d. Message routing schemes.

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2002 SCHEME

CS82

Eighth Semester B.E. Degree Examination, Dec.09-Jan.10
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With relevant block diagram, discuss any two Shared-Memory multiprocessor models. **(08 Marks)**

b. With neat block diagram explain the classification of computer architecture based on the notions of number of instruction and data streams. **(06 Marks)**

c. Consider the execution of an object code with two million instructions on a 40 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment :

Sl.No.	Instruction Type	CPI	Instruction mix
1	Arithmetic and logic	1	60%
2	Load/store with cache hit	2	18%
3	Branch	4	12%
4	Memory reference with cache miss	8	10%

Table.Q1(c)

i) Calculate the average CPI when the program is executed on a uni-processor with the above trace results.

ii) Calculate the corresponding MIPS rate based on the CPI obtained in (i) **(06 Marks)**

2 a. Represent a three-dimensional binary cube of eight nodes and discuss the three routing functions based on the three bits in the node address. List any three factors that affect the performance of an interconnection network. **(10 Marks)**

b. Define Flow dependence and Anti-dependence. **(04 Marks)**

c. Analyze the data dependences among the following statements in a given program :

```
S1:  Load   R1, 1024          / R1← 1024 /
S2:  Load   R2, M(10)         / R2← Memory (10) /
S3:  Add    R1, R2            / R1← (R1) + (R2) /
S4:  Store  M(1024), R1       / Memory (1024) ← (R1) /
S5:  Store  M((R2)), 1024     / Memory (64) ← (1024) /
```

Where (Ri) means content of register Ri and Memory(10) contains 64 initially.

i) Draw a dependence graph to show all the dependences.

ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU? **(06 Marks)**

3 a. Draw and explain a typical VLIW processor architecture and its instruction format. Explain its pipeline operation (with degree m = 3) using timing diagram. **(10 Marks)**

b. With a neat block diagram explain the interleaved memory organization that support block access in a pipelined fashion. Using a suitable timing chart, indicate the major and minor cycle and effective access time. **(10 Marks)**

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CS8

4 a. In connection with instruction pipelines, explain the static and dynamic branch predictio schemes. Represent the BTB organization. **(08 Marks)**

b. Consider the following non-linear pipeline reservation table :

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

Table.Q4(b)

i) List the set of forbidden latencies and initial collision vector.
ii) Draw the state transition diagram
iii) List all simple cycles and greedy cycles.
iv) Determine the optimal constant latency cycle and MAL. **(08 Marks)**

c. A non-pipelined processor X has a clock rate of 25 MHz and an average CPI of 4. Processor Y, an improved successor of X, is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 20 MHz.
i) If a program containing 100 instructions is executed on both processors, what is the speedup of processor Y compared with that of processor X?
ii) Calculate the MIPS rate of each processor during the execution of this particular program. **(04 Marks)**

5 a. Draw a 8-input Omega network using 2 x 2 switches. Show the switch settings for achieving routing permutation $\pi = (0, 7, 6, 4, 2)\ (1, 3)\ (5)$. Is there any conflict in the switch settings to implement this permutation? **(10 Marks)**

b. What is cache coherence? Explain the concept of bus snooping to maintain the coherence. **(10 Marks)**

6 a. Discuss in detail, the different steps in the parallelization process. **(10 Marks)**

b. Describe the simulation of Ocean current and justify the need for multiprocessing for this problem. **(10 Marks)**

7 a. Discuss synchronous and Asynchronous message passing protocols. **(10 Marks)**

b. Discuss control flow and data flow architecture. **(10 Marks)**

8 Write short notes on :

a. Pipeline for fixed-point multiplication of 8-bit integers. **(06 Marks)**

b. Vector supercomputer **(07 Marks)**

c. Hierarchical bus system. **(07 Marks)**

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2002 SCHEME CS82

Eighth Semester B.E. Degree Examination, Dec.08 / Jan.09
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain the Flynn's classification of computer architecture. (08 Marks)

b. Explain the following terms related to system attributes to performance: i) Clock rate and CPI ii) MIPS rate iii) Performance factor (06 Marks)

c. A 40 MHz processor was used to execute benchmark program with the following instruction mix and clock cycle counts.

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time. (06 Marks)

2 a. Explain Grain packing and scheduling for parallel programming with example. (10 Marks)

b. What is dynamic connection N/W? Design the 16×16 omega N/W. (10 Marks)

3 a. Explain in detail the 1EEE Future bus + Back plane bus standard specification. (10 Marks)

b. Describe the Daisy chaining and the distributed arbiter for bus arbitration in a multiprocessor system. State the advantages and disadvantages of each case from both implementational and operational point of view. (10 Marks)

4 a. Consider the following reservation table:

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

i) What are the forbidden latencies?
ii) Draw a transition diagram.
iii) List all the greedy cycles and simple cycles.
iv) What is optimal constant latency?
v) What is minimal average latency? (10 Marks)

b. What is the distinction between Carry Propogate Adder (CPA) and Carry Save Adder (CSA)? Explain with an example. (05 Marks)

c. Explain the pipeline unit per fixed point multiplication of 8-bit integer. (05 Marks)

5 a. Explain the mechanism for instruction pipelining. (10 Marks)

b. In connection with instruction pipeline explain the following:
i) Dynamic instruction scheduling. ii) Branch handling techniques. (10 Marks)

6 a. What is cache coherence? Explain the concept of bus snooping by cache coherence to maintain coherence. (10 Marks)

b. Explain the directory-based protocols for network-connected system. (10 Marks)

7 a. Explain the steps involved in parallelization process. (08 Marks)

b. Explain Orchestration under the data parallel model for the case of data parallel equation solver. Also write the pseudo code for the same. (12 Marks)

8 Write short notes on:
a. VLIW Architecture.
b. Bandwidth scaling.
c. Shared memory multiprocessor.
d. Vector super computers. (20 Marks)

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06CS81

Eighth Semester B.E. Degree Examination, May/June 2010
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. What is dependability? Explain two main measures of dependability. **(06 Marks)**

c. Given the following measurements:

Frequency of FP operations = 25% Average CPI of FP operations = 4.0

Average CPI of other instructions = 1.33 Frequency of FPSQR = 2%

CPI of FPSQR = 20

Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare the two design alternatives using the processor performance equations. **(06 Marks)**

2 a. With a neat diagram, explain the classic five-stage pipeline for a RISC processor. **(10 Marks)**

b. What are the major hurdles of pipelining? Illustrate the branch hazards in detail. **(10 Marks)**

3 a. What are the techniques used to reduce branch costs? Explain both static and dynamic branch prediction used for same. **(10 Marks)**

b. With a neat diagram, give the basic structure of Tomasulo based MIPS FP unit and explain the various fields of reservation stations. **(10 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(10 Marks)**

b. What are the key issues in implementing advanced speculation techniques? Explain them in detail. **(10 Marks)**

PART – B

5 a. Explain the basic schemes for enforcing coherence in a shared memory multiprocessor system. **(10 Marks)**

b. Explain the directory based coherence for a distributed memory multiprocessor system. **(10 Marks)**

6 a. Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the mass penalty is 25 clock cycles and the mass rate is 2%, how much faster would the computer be if all instructions were cache hits? **(10 Marks)**

b. Explain in brief, the types of basic cache optimization. **(10 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. **(10 Marks)**

b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. **(10 Marks)**

8 a. Explain in detail, the hardware support for preserving exception behaviour during speculation. **(10 Marks)**

b. Explain the prediction and speculation support provided in IA64. **(10 Marks)**

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